CLAIMS

The following is a detailed listing of all claims that are, or were, in the Application.

1. (Previously presented) A method for driving a data signal comprising:

providing a plurality of bit lines;

providing a data bus having a plurality of bus lines, wherein each bus line is connectable to a respective portion of a plurality of bit lines; and

pre-charging at least one of the bus lines of the data bus to a first voltage level in advance of driving a first type of data signal or a second type of data signal across the at least one of the bus lines.

2. (Previously presented) The method of claim 1, wherein the first type of data signal is a high data signal; and the second type of data signal is a low data signal.

3. (Original) The method of claim 1, wherein the first voltage level is about 1.8 Volts.

4. (Original) The method of claim 1, wherein the first level voltage level corresponds to a power supply voltage level.

5. (Original) The method of claim 1, wherein the first type of data signal corresponds to the binary digit "1".

6. (Previously presented) The method of claim 22, wherein maintaining the at least one of the bus lines of the data bus at the first level comprises connecting the at least one of the bus lines of the data bus to a power supply voltage source.

7. (Previously presented) The method of claim 22, wherein maintaining the at least one of the bus lines of the data bus at the first level comprises connecting the at least one of the bus lines of the data bus to ground.

8. (Original) The method of claim 1, wherein the second voltage level is about 0.0 Volts.

9. (Original) The method of claim 1, wherein the second type of data signal corresponds to the binary digit "0".

10. (Previously presented) The method of claim 23, wherein pulling the at least one of the bus lines of the data bus to the second voltage level comprises connecting the at least one of the bus lines of the data bus to a power supply voltage source.

11. (Previously presented) The method of claim 23, wherein pulling the at least one of the bus lines of the data bus to the second voltage level comprises connecting the at least one of the bus lines of the data bus to ground.

12. (Previously presented) The method of claim 23, wherein pulling the at least one of the bus lines of the data bus to a second voltage level comprises turning on a transistor so that current flows through the transistor from the at least one of the bus lines of the data bus to ground.

13. (Previously presented) The method of claim 23, wherein pulling the at least one of the bus lines of the data bus to a second voltage level comprises turning on a transistor so that current flows through the transistor from a power supply voltage source to the at least one of the bus lines of the data bus.

14. (Previously presented) A system for driving a data signal, comprising:

a plurality of bit lines;

a data bus having a plurality of bus lines, wherein each bus line is connectable to a respective portion of the plurality of bit lines; and

a charging circuit coupled to at least one of the bus lines of the data bus, wherein the charging circuit is configured to pre-charge the at least one of the bus lines of the data bus to a first voltage level in advance of driving a first type of data signal or a second type of data signal across the at least one of the bus lines.

15. (Previously presented) The system of claim 14, further comprising a keeper circuit coupled to the at least one of the bus lines of the data bus, wherein the keeper circuit is configured to maintain the at least one of the bus lines of the data bus at the first voltage level after the at least one of the bus lines of the data bus has been charged.

16. (Previously presented) The system of claim 24, wherein the pull-down circuit comprises:

a transistor coupled at one end to the at least one of the bus lines of the data bus and at the other end to ground;

logic circuitry coupled to a gate of the transistor, wherein an output signal from the logic circuitry controls the transistor.

17. (Original) The system of claim 16 wherein the logic circuitry comprises a first input terminal for receiving an equilibration signal and a second input terminal for receiving a data signal.

18. (Previously presented) The system of claim 16, wherein the logic circuitry comprises a NOR gate.

19. (Previously presented) The system of claim 14, wherein the charging circuit comprises:

a transistor coupled at one end to a power supply voltage source and at the other end to the at least one of the bus lines of the data bus, wherein the transistor is controlled by an equilibration signal.

20. (Previously presented) The system of claim 15, wherein the keeper circuit comprises:

a transistor coupled at one end to a power supply voltage source and at the other end to the at least one of the bus lines of the data bus; and

logic circuitry coupled to a gate of the transistor, wherein an output signal from the logic circuitry controls the transistor.

21. (Original) The system of claim 20, wherein the logic circuitry comprises an inverter gate.

22. (Previously presented) The method of claim 1, comprising maintaining the at least one of the bus lines of the data bus at the first voltage level when the first type of data signal is to be driven across the at least one of the bus lines of the data bus

23. (Previously presented) The method of claim 1, comprising pulling the at least one of the bus lines of the data bus to a second voltage level when a second type of data signal is to be driven across the at least one of the bus lines of the data bus.

24. (Previously presented) The system of claim 14, comprising a pull-down circuit coupled to the at least one of the bus lines of the data bus, wherein the pull-down circuit is configured to pull the at least one of the bus lines of the data bus to a second voltage level.